



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/543,166	07/22/2005	Hideki Yamanaka	ISH-0234	7946
23353	7590	05/09/2007	EXAMINER	
RADER FISHMAN & GRAUER PLLC			ABOULFAIDA, AMBER	
LION BUILDING			ART UNIT	PAPER NUMBER
1233 20TH STREET N.W., SUITE 501			2809	
WASHINGTON, DC 20036			MAIL DATE	DELIVERY MODE
			05/09/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)
	10/543,166	YAMANAKA ET AL.
	Examiner	Art Unit
	Amber V. Aboufaida	2809

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 28 November 2005.
- 2a) This action is FINAL. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-9 is/are pending in the application.
 - 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 1-9 is/are rejected.
- 7) Claim(s) _____ is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on 22 July 2005 is/are: a) accepted or b) objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 - a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.



AB 2897
05.07.2007

Attachment(s)

- | | |
|----------------------------------------------------------------------------------------|-------------------------------------------------------------------|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date: _____ |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date <u>11/28/05, 07/22/05</u> | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

This office action is in response to the IDS filed 11/28/05 and to application, 10/543,166, filed on 7/22/05, which is a 371 of PCT/JP04/00869, filed on 01/29/04.

Currently claims 1-9 are pending.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 2, 3, 6, and 8 are rejected under 35 U.S.C. 102(b) as being anticipated by Kizuki et al., US 5,882,952, dated March 16, 1999.

Pertaining to **claim 1**, Kizuki et al. show a silicon semiconductor substrate (col. 7, lines 49-52; It is the examiner's position that the SiO₂ layer serves as a substrate to the active layer, 96.) comprising: a {110} plane or a plane inclined from a {110} plane as a main surface of the substrate (col. 2, lines 39-41); and steps arranged at an atomic level along a <110> orientation on the main surface (col. 2, line 50).

Pertaining to **claim 2**, Kizuki et al. show the silicon semiconductor substrate according to claim 1, wherein the plane inclined from the {110} plane is a plane inclined from the {110} plane toward a <100> orientation (col. 2, line 40-41; It is the examiner's position that a <100> direction encompasses [100], [010], [001], etc.).

Pertaining to **claim 3**, the silicon semiconductor substrate according to claim 2, wherein a silicon single crystal thin film is formed by means of an epitaxial growth method on the surface of the silicon semiconductor substrate having the plane inclined from the {110} plane as the main surface (col. 7, lines 37, and 45).

Pertaining to **claim 6**, the silicon semiconductor substrate according to claim 2, wherein an inclination angle of the silicon semiconductor substrate having the plane inclined from the {110} plane toward the <100> orientation as the main surface is 0 degree or more and less than 8 degrees (col. 5, lines 1-4).

Pertaining to **claim 8**, a method for manufacturing a silicon semiconductor substrate, which is the silicon semiconductor substrate according to claim 2, comprising the steps of: preparing a silicon semiconductor substrate having a plane inclined from a {110} plane toward a <100> orientation as a main surface (col. 2, lines 39-41, (col. 2, line 40-41; It is the examiner's position that a <100> direction encompasses [100], [010], [001], etc.)); and growing a silicon single crystal thin film by means of an epitaxial growth method on the main surface (col. 7, lines 37, and 45).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

- (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 4 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kizuki et al. as applied to claims 1 and 2 above, and further in view of Bedell et al., US 2006/0148143, effectively filed, 01/06/05.

Kizuki et al. show claim 2 substantially.

Kizuki et al. lack anticipation only, pertaining to claims 4 and 9, in failing to show that the main surface is subjected to heat treatment in a hydrogen gas atmosphere, an argon gas atmosphere or an atmosphere of a mixture thereof.

Bedell et al. teach, in paragraph [0030], lines 7-9, an annealing step carried out in an inert atmosphere such as He, Ar, Ne, or a mixture thereof.

It would have been obvious to one of ordinary skill in the art, at the time the invention was made, pertaining to claims 4 and 9, to have the {110} substrate of Kizuki be subjected to heat treatment in a hydrogen gas atmosphere, an argon gas atmosphere or an atmosphere of a mixture thereof, as taught by Bedell, with the motivation that the heat treatment would smooth the surface, thus increasing electron mobility. Since Bedell show a substrate with a {110} orientation, the expectation of success of having the substrate of Kizuki be subjected to a heat treatment in a hydrogen gas atmosphere, an argon gas atmosphere or an atmosphere of a mixture thereof, as taught by Bedell, is reasonable.

Claims 5 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kizuki et al. as applied to claims 1 and 2 above, and further in view of Mitani et al., US 2005/0003648, effectively filed 12/25/02.

Kizuki et al. show, pertaining to **claim 5**, a silicon semiconductor substrate (col. 7, lines 49-52; It is the examiner's position that the SiO₂ layer serves as a substrate to the active layer, 96.) having a plane inclined from a {100} plane toward a <100> orientation as a main surface (col. 2, line 40-41; It is the examiner's position that a <100> direction encompasses [100], [010], [001], etc.); pertaining to **claim 7**, claim 2 substantially.

Kizuki et al. lack anticipation only, in failing to show, pertaining to claim 5, that the surface of the silicon semiconductor substrate is mirror polished; pertaining to claim 7, that an orientation flat or a notch is formed in the <110> orientation.

Mitani et al. teach, pertaining to **claim 5**, a mirror polished silicon wafer having a crystal plane orientation of {110} ([0045], lines 3-4); pertaining to **claim 7**, an orientation flat formed in a direction of [-110] on the (110) plane of the first silicon single crystal wafer ([0055], lines 8-10).

It would have been obvious to one of ordinary skill in the art, at the time the invention was made, pertaining to **claim 5**, to have the substrate of Kizuki be mirror polished, as taught by Mitani, with the motivation that a mirror polished and cleaned surface of a silicon wafer having a specific crystal plane can lower warpage due to a heat treatment. Since Kizuki has a substrate with a {110} orientation, the expectation of success of having the substrate be mirror polished, as taught by Mitani, is reasonable.

It would have been obvious to one of ordinary skill in the art, at the time the invention was made, pertaining to **claim 7**, to have the substrate of Kizuki contain an orientation flat or notch formed in the <110> orientation, as taught by Mitani, with the motivation that channel mobility can be easily improved, and that the bonded wafer can be easily made into chips. Since

Art Unit: 2809

Kizuki has a substrate with a {110} orientation, the expectation of success of having the substrate contain an orientation flat or notch formed in the <110> orientation, as taught by Mitani, is reasonable.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Amber V. Aboufaida whose telephone number is (571)-270-1558. The examiner can normally be reached on Monday through Friday 7:30 AM - 5:00 PM E.S.T..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Gurley can be reached on 571-272-1670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

A.A.
May 3, 2007

P.A. C.Y. *av 2827*
05.07.2007